WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate;

a pair of first diffusion layers formed within said semiconductor substrate;

a gate insulating film formed on that portion of said semiconductor substrate which is positioned between said paired diffusion layers;

a gate electrode including a first gate portion formed on said gate insulating film and a second gate portion formed on said first gate portion, a first width in a channel direction of said first gate portion being substantially equal to a width in said channel direction of said gate insulating film, and a second width in said channel direction of said second gate portion being larger than said first width;

a gate side wall insulating film including a first side wall portion formed on a side surface of said first gate portion and on a side surface of said gate insulating film and a second side wall portion formed on a side surface of said second gate portion; and

a second diffusion layer formed apart from said first diffusion layers within that portion of said semiconductor substrate which is positioned below said gate insulating film.

2. A semiconductor device, comprising:

a semiconductor substrate;

a pair of first diffusion layers formed within said semiconductor substrate;

a gate insulating film including a first insulating film portion formed on that portion of said semiconductor substrate which is positioned between said first diffusion layers and a second insulating film portion positioned on both edges of said first insulating film portion, a thickness of said second insulating film portion being larger than a thickness of said first insulating film portion;

a gate electrode formed on said gate insulating film;

a gate side wall insulating film formed on a side surface of said gate electrode and on a side surface of said second insulating film portion; and

a second diffusion layer formed apart from said first diffusion layers within that portion of said semiconductor substrate which is positioned below said first insulating film portion.

3. The semiconductor device according to claim 1, further comprising a third diffusion layer including a first diffusion portion formed below said first diffusion layers under said first side wall portion and a second diffusion portion formed below said second diffusion layer, a distance of a peak portion of a impurity concentration in said first diffusion portion from a surface of said semiconductor substrate being

larger than a distance of a peak portion of a impurity concentration in said second diffusion portion from the surface of said semiconductor substrate.

4. The semiconductor device according to claim 1, wherein said first diffusion layers further comprises:

a pair of extension regions formed below said second side wall portion apart from said second diffusion layer; and

a pair of source-drain regions formed in contact with said extension regions on a side opposite said second diffusion layer.

5. The semiconductor device according to claim 2, wherein said first diffusion layers further comprises:

a pair of extension regions formed below said gate side wall insulating film apart from said second diffusion layer; and

a pair of source-drain regions formed in contact with said extension regions on a side opposite said second diffusion layer.

6. The semiconductor device according to claim 2, wherein said gate side wall insulating film comprises:

a third side wall portion formed on the side surface of said gate electrode and on the side surface of said second insulating film portion; and

a fourth side wall portion formed on a side surface of said third side wall portion.

7. The semiconductor device according to claim 1,

further comprising an interlayer insulating film formed to surround said gate side wall insulating film, an upper surface of said interlayer insulating film being substantially equal to an upper surface of said gate electrode.

8. The semiconductor device according to claim 2, further comprising an interlayer insulating film formed to surround said gate side wall insulating film, an upper surface of said interlayer insulating film being substantially equal to an upper surface of said gate electrode.

9. The semiconductor device according to claim 1, wherein a conductivity type of said second diffusion layer is opposite the conductivity type of said semiconductor substrate.

10. The semiconductor device according to claim 2, wherein a conductivity type of said second diffusion layer is opposite the conductivity type of said semiconductor substrate.

11. The semiconductor device according to claim 3, wherein a conductivity type of said third diffusion layer is equal to the conductivity type of said semiconductor substrate.

12. The semiconductor device according to claim 1, wherein said gate insulating film is thicker than said first side wall portion.

13. A method of manufacturing a semiconductor

device, comprising:

forming a first material layer on a semiconductor substrate;

forming a second material layer comprising a first width on said first material layer;

partly removing said first material layer to leave said first material layer comprising a second width smaller than said first width below said second material layer;

introducing an impurity into said semiconductor substrate with said second material layer used as a mask to form an extension region;

forming a gate side wall insulating film on a side surfaces of said first and second material layers, said gate side wall insulating film including a first side wall portion formed on the side surface of said first material layer and a second side wall portion formed on the side wall of said second material layer;

introducing an impurity into said semiconductor substrate with said gate side wall insulating film and said second material layer used as a mask to form source and drain regions;

forming an interlayer insulating film on said semiconductor substrate, on said second material layer and on said gate side wall insulating film, followed by removing said interlayer insulating film until said second material layer is exposed;

removing said first and second material layers to form a groove;

introducing an impurity through said groove into said semiconductor substrate to form a second diffusion layer apart from said extension region within that portion of said semiconductor substrate which is positioned below said groove;

forming a gate insulating film on that portion of said semiconductor substrate which is positioned within said groove; and

forming a gate electrode on said gate insulating film positioned within said groove.

14. A method of manufacturing a semiconductor device, comprising:

forming a gate insulating film on a semiconductor substrate;

forming a second material layer comprising a predetermined shape on said gate insulating film;

thermally oxidizing said second material layer and said semiconductor substrate to form a first insulating film on an upper surface and a side surface of said second material layer and to increase a thickness in a portion of said gate insulating film;

partly removing said first insulating film and said gate insulating film to form a first gate side wall insulating film on the side surface of said second material layer and to form a second insulating film

portion of said gate insulating film positioned below both edges of said second material layer comprising a thickness larger than a thickness of the first insulating film portion of said gate insulating film below a central portion of said second material layer;

introducing an impurity into said semiconductor substrate with said second material layer and said first gate side wall insulating film used as a mask to form an extension region;

forming a second gate side wall insulating film on a side surface of said first gate side wall insulating film;

introducing an impurity into said semiconductor substrate with said second material layer and said first and second gate side wall insulating films used as a mask to form source-drain regions;

forming an interlayer insulating film on said semiconductor substrate, said second material layer and said first and second gate side wall insulating films, followed by removing said interlayer insulating film until said second material layer is exposed;

removing said second material layer to form a groove;

introducing an impurity through said groove into said semiconductor substrate to form a second diffusion layer apart from said extension region within that portion of said semiconductor substrate which is

positioned below said first insulating film portion; and

forming a gate electrode on said gate insulating film positioned within said groove.

15. The method of manufacturing a semiconductor device according to claim 13, further comprising forming a third diffusion layer below said extension region and said second diffusion layer by introducing an impurity through said groove into said semiconductor substrate after formation of said second diffusion layer.

16. The method of manufacturing a semiconductor device according to claim 15, wherein said third diffusion layer includes a first diffusion portion formed below said extension region and a second diffusion portion formed below said second diffusion layer, a distance of a peak portion of the impurity concentration in said first diffusion portion from a surface of said semiconductor substrate being smaller than a distance of a peak portion of the impurity concentration in said second diffusion portion from the surface of said semiconductor substrate.

17. The method of manufacturing a semiconductor device according to claim 13, wherein a conductivity type of said second diffusion layer is opposite the conductivity type of said semiconductor substrate.

18. The method of manufacturing a semiconductor

device according to claim 14, wherein a conductivity type of said second diffusion layer is opposite the conductivity type of said semiconductor substrate.

19. The method of manufacturing a semiconductor device according to claim 15, wherein a conductivity type of said third diffusion layer is equal to the conductivity type of said semiconductor substrate.

20. The method of manufacturing a semiconductor device according to claim 14, wherein said first material layer is thicker than said gate insulating film.

21. The method of manufacturing a semiconductor device according to claim 13, wherein said gate insulating film is thinner than said first side wall portion.